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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/760,509	01/12/2001	Gilbert Wolrich	10559/317001/P9678	2157

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EXAMINER	
O BRIEN, BARRY J	

ART UNIT	PAPER NUMBER
2183	5

DATE MAILED: 03/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/760,509	WOLRICH ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/12/01, 4/24/01 and 12/16/02*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-29 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Declaration as received on 4/24/2001 and Change of Address as received on 12/16/2002.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

5. The disclosure is objected to because of the following informalities: The specification lacks "Summary" section or general statement of the invention as set forth in 37 CFR 1.73. The summary is separate and distinct from the abstract and is directed toward the invention rather than the disclosure as a whole. The summary may point out the advantages of the invention or how it solves problems previously existent in the prior art (and preferably indicated in the Background of the Invention). In chemical cases it should point out in general terms the utility of the invention. If possible, the nature and gist of the invention or the inventive concept should

be set forth. Objects of the invention should be treated briefly and only to the extent that they contribute to an understanding of the invention. See MPEP § 608.01(d). See the below paragraphs regarding proper the inclusion of a summary section.

6. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or
REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)
(e) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(f) BRIEF SUMMARY OF THE INVENTION.
(g) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(h) DETAILED DESCRIPTION OF THE INVENTION.
(i) CLAIM OR CLAIMS (commencing on a separate sheet).
(j) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(k) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Appropriate correction is required.

Claim Objections

7. Claim14 is objected to because of the following informalities: The claim contains the limitation "...a ctx_enable register **and with** execution of the context swap instruction specifying a kill operation **causing** the ctx_enable bit to be set..." on its third line. This claim language is grammatically incorrect English. Please correct the language to read more similar to, "...a ctx_enable register, **wherein** the execution of a context swap instruction specifying a kill operation **causes** the ctx_enable bit to be set..." Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claims 10 and 11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

10. Claim 10 recites the limitation "a sequence number change" on its second line. Page 19 of specification states, "the parameter can also be specified as 'seq_num1_change/seq_num2_change', which swaps out the current context and wakes it up when the value of the sequence number changes." This does not enable one of ordinary skill in the art to make or use the invention, as it does not define what a sequence number or a sequence number change is, or what changes the sequence number. For the purposes of this examination,

the Examiner will assume that a "sequence number change" refers to a round-robin type counter that updates every time a thread switch occurs, which has a sequence of numbers that change to indicate that a context switch is required (see paragraph 44 below).

11. Claim 11 recites the limitation "an inter-thread signal input" on its second line. Page 19 simply states, "the parameter can be specified as 'inter_thread' which swaps out the current context and wakes it up when the threads interthread signal is received." This does not enable one of ordinary skill in the art to make or use the invention, as it does not define what the interthread signal represents, or how it differs from another parameter specifier, for example the SRAM signal, which also swaps out the current context and wakes up the thread when a signal is received. For the purposes of this examination, the Examiner will assume that "an inter_thread signal input" refers to a signal relating between two or more threads (see paragraph 47 below).

12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

13. Claims 1, 8-12, 14 and 27 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

14. Claim 1 recites the limitation, "the register set constructed with a two-ported random access memory, with the register set divided into a plurality of banks and with two different words from each bank of the register set can be read and written in the same processor cycle." This limitation is unclear. It is unclear how a single two-ported register file, which can perform at most two accesses per cycle, can perform four accesses (two per bank) each cycle as defined by the limitation "two different words from each bank...can be read and written in the same

processor cycle." It is also unclear how the limitation performs eight accesses (four per bank), with the accesses being interpreted as two words per read and two words per write per bank, clearly requiring 8 ports, even though the register file is created from a single two port RAM. For the purposes of this examination, the Examiner will assume that the entire register file, including both banks, can perform at most two accesses, as dictated by the claimed two-port register file, in one processor cycle (see paragraph 21 below).

15. Claim 8 recites the limitations "unavailable thread memory set" and "available thread memory set in its second and third lines, respectively. There is insufficient antecedent basis for this limitation in the claim or in the specification. Also see claims 9-12, which are dependent upon claim 8, that also contain the said limitations.

16. Furthermore, the limitations "available thread memory set" and "unavailable thread memory set" are unclear. The examiner assumes that these limitations refer to the "set of memory locations for storing a list of available threads that correspond to threads that are ready to be executed", and "a set of memory locations for storing a list of unavailable threads that are not ready to be executed", respectively, of claim 7. However, it is unclear whether the limitations of claim 8 refer to the "set of memory locations" or the "list of unavailable/available threads", as the language of claim 8 implies that a context of a currently running thread is to be saved into the unavailable thread memory set, but the unavailable thread memory set stores a list of unavailable threads, not a context, as defined in claim 7. The same goes for the execution of a thread from the available thread memory set, as it contains a list, not a thread context. Again, also see claims 9-12, which are dependent upon claim 8, for more examples of the above limitations that require correction.

17. Claim 10 recites the limitation "sequence number change" in its second line. There is insufficient antecedent basis for this limitation in the specification. While page 19 of the specification discuses the situation "when the value of the sequence number changes," it does not discuss a "sequence number change." Thus, the limitation lacks antecedent basis in the specification.

18. Claim 14 recites the limitation "ctx_enable bit" in its fourth line. There is insufficient antecedent basis for this limitation in the claim. See also similar antecedent basis problem in claim 27.

Claim Rejections - 35 USC § 102

19. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

20. Claims 1-5 and 15-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Parady, U.S. Patent No. 5,933,627.

21. Regarding claims 1 and 15, taking claim 1 as exemplary, Parady has taught an execution unit for execution of multiple context threads comprises:

a. An arithmetic logic unit to process data for executing threads (see Col.2 lines 18-29 and Col.3 lines 19-25),

b. Control logic to control the operation of the arithmetic logic unit (see Col.3 lines 10-18),

c. A general purpose register set to store and obtain operands for the arithmetic logic unit, the register set constructed with a two-ported random access memory (48 of Fig.1/Fig.3), with the register set divided into a plurality of banks (see Col.3 lines 43-49) and with two different words from each bank of the register set can be read and written in the same processor cycle (see Fig.3 and Col.3 lines 43-49). Here, because the register file contains ten ports (see 48 of Fig.1) and four banks (see Col.3 lines 43-49), there are inherently at least two ports per bank, therefore allowing each bank to write or read at least one word per bank per cycle (see above paragraph 14).

22. Claim 15 is nearly identical to claim 1, differing in its parent claim, but encompassing the same scope. Therefore, claim 15 is rejected for the same reasons as claim 1.

23. Regarding claims 2 and 16, taking claim 2 as exemplary, Parady has taught the execution unit of claim 1, wherein the register set is logically partitioned into a plurality of relatively addressable windows (see Col.3 lines 43-49 and Col.4 lines 1-8). Here, the register file is divided into four register files for four threads (see Col.3 lines 43-45), and there is a thread field in each instruction that identifies which thread an instructions operands come from (see Col.4 lines 1-8). This makes each register in each register file relatively addressable, being differentiated from each other relative to their 2-bit thread field.

24. Claim 16 is nearly identical to claim 2, differing in its parent claim, but encompassing the same scope. Therefore, claim 16 is rejected for the same reasons as claim 2.

25. Regarding claims 3 and 17, taking claim 3 as exemplary, Parady has taught the execution unit of claim 2, wherein the number of windows of the register set is according to the number of threads that can execute in the processor (see Col.3 lines 43-49).

26. Claim 17 is nearly identical to claim 3, differing in its parent claim, but encompassing the same scope. Therefore, claim 17 is rejected for the same reasons as claim 3.

27. Regarding claims 4, 18 and 21, taking claim 4 as exemplary, Parady has taught the execution unit of claim 1, where the relative addressing allows the currently executing thread to access to any of the registers relative to the starting point of a window of registers (see Col.3 lines 43-49 and Col.4 lines 1-8). Here, the register file is divided into four register files for four threads (see Col.3 lines 43-45), and there is a thread field in each instruction that identifies which thread an instructions operands come from (see Col.4 lines 1-8). This makes each register in each register file relatively addressable, being differentiated from each other relative to their 2-bit thread field, allowing a thread to access registers associated with its 2-bti thread field.

28. Claims 18 and 21 are nearly identical to claim 4, differing in their parent claims, but encompassing the same scope. Therefore, claim 18 and 21 are rejected for the same reasons as claim 4.

29. Regarding claims 5 and 22, taking claim 5 as exemplary, Parady has taught the execution unit of claim 1, wherein the register set is absolutely addressable where any one of the addressable registers may be accessed by the currently executing thread by providing the exact address of the register (see Col.3 lines 43-49 and Col.4 lines 1-8, 18-22). As shown above in paragraphs 23 and 27, the register set is relatively addressable using a 2-bit thread field that specifies which thread, and consequently which register window, an instruction's operands come

from. However, the 2-bit thread field can also be used to inter-relate two threads (see Col.4 lines 18-22), thus allowing one thread to access to any other register in any other thread, providing absolute addressability.

30. Claim 22 is nearly identical to claim 5, differing in its parent claim, but encompassing the same scope. Therefore, claim 22 is rejected for the same reasons as claim 5.

31. Regarding claim 19, Parady has taught a processor unit comprising:

a. An execution unit for execution of multiple context threads comprising:

a. An arithmetic logic unit to process data for executing threads (see Col.2 lines 18-29 and Col.3 lines 19-25),

b. Control logic to control the operation of the arithmetic logic unit (see Col.3 lines 10-18),

c. A general purpose register set (48 of Fig.1/Fig.3) to store and obtain operands for the arithmetic logic unit (see Fig.3), the register set constructed with a two-ported random access memory. While not taught explicitly, it is inherent in the operation of a register file that it has at least one port to read and one port to write data in and out of the register file, and thus inherently a register file has at least two ports.

32. Regarding claim 20, Parady has taught the processor of claim 19, wherein the register set is logically partitioned into a plurality of relatively addressable windows where the number of windows of the register set is according to the number of threads that can execute in the processor (see Col.3 lines 43-49 and Col.4 lines 1-8). Here, the register file is divided into four register files for four threads (see Col.3 lines 43-45), and there is a thread field in each

instruction that identifies which thread an instructions operands come from (see Col.4 lines 1-8). This makes each register in each register file relatively addressable, being differentiated from each other relative to their 2-bit thread field.

Claim Rejections - 35 USC § 103

33. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

34. Claims 6-10, 23-25 and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627 as applied to claims 1-5 above, and further in view of Waldspurger et al., "*Register Relocation: Flexible Contexts for Multithreading*".

35. Regarding claims 6 and 23, taking claim 6 as exemplary, Parady has taught the execution unit of claim 1, wherein the control logic further comprises:

a. Context switching logic (112 of Fig.3) fed by signals from a plurality of shared resources (see Col.3 lines 57-65).

36. Parady has not explicitly taught wherein the signals cause the context event logic to indicate that threads are either available or unavailable for execution.

37. However, Waldspurger has taught a context switch scheduler that comprises a circularly-linked "ready queue" which determines which contexts are ready for execution when a context switch is required in order to provide fast context switching (see paragraph 1 of Sec. 2.2). One of ordinary skill in the art would have recognized that it is a primary goal of microprocessor

designers to reduce delays in their datapath, such as those introduced when a context switch is required, thereby increasing the speed and throughput of their processors. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to provide threads that are available for execution in the manner of Waldspurger so that context switches can be performed fast, thus increasing the processor speed.

38. Regarding claims 7 and 23, taking claim 7 as exemplary, Parady in view of Waldspurger has taught the execution unit of claim 6, wherein the control logic addresses a set of memory locations for storing a list of available threads that correspond to threads that are ready to be executed and a set of memory locations for storing a list of unavailable threads that are not ready to be executed (see above paragraph 37 and Waldspurger paragraph 1 of Sec. 2.2). Here, the "set of memory locations" is a circularly-linked queue, such that the next threads that are ready to be executed are at the "head" of the list, while those that are not ready, or were recently switched from, reside at the "tail" of the list (see Waldspurger Sec. 2.2).

39. Claim 23 is nearly identical to claims 6 and 7, differing in its parent claim, but encompassing the same scope as claims 6 and 7. Therefore, claim 23 is rejected for the same reasons as claims 6 and 7.

40. Regarding claims 8, 24 and 28, taking claim 8 as exemplary, Parady in view of Waldspurger has taught the execution unit of claim 7, wherein execution of a context swap instruction causes a currently running thread to be swapped out to the unavailable thread memory set and a thread from the available thread memory set to begin execution within a single execution cycle (see Parady Fig.3, Col.2 lines 18-25, Col.3 lines 57-65 and Waldspurger paragraphs 2-5 of Sec. 2.2.). Here, a load or store operation signals a context switch (see Parady

Fig.3 and Col.3 lines 57-65), and the context switch steps store the current context at the "tail" of the circularly-linked list and update the current context to be the thread that was next in line to be executed (see Waldspurger paragraphs 2-5 of Sec. 2.2).

41. Claims 24 and 28 are nearly identical to claim 8, differing in their parent claims, but encompassing the same scope. Therefore, claims 24 and 28 are rejected for the same reasons as claim 8.

42. Regarding claims 9, 25 and 29, taking claim 9 as exemplary, Parady in view of Waldspurger has taught the execution unit of claim 8, wherein execution of the context swap instruction specifies one of the signal inputs and upon receipt of the specified signal input causes the swapped out thread to be stored in the available thread memory set (see Parady Fig.3, Col.2 lines 18-25, Col.3 lines 57-65 and Waldspurger paragraphs 2-5 of Sec. 2.2.). Here, a load or store operation signals a context switch (see Parady 114 of Fig.3 and Col.3 lines 57-65), and the context switch steps store the current context at the "tail" of the circularly-linked list and update the current context to be the thread that was next in line to be executed (see Waldspurger paragraphs 2-5 of Sec. 2.2).

43. Claims 25 and 29 are nearly identical to claim 9, differing in their parent claims, but encompassing the same scope. Therefore, claims 25 and 29 are rejected for the same reasons as claim 9.

44. Regarding claim 10, Parady in view of Waldspurger has taught the execution unit of claim 8, wherein execution of the context swap instruction specifies a sequence number change and upon receipt of the specified sequence number change causes the swapped out thread to be stored in the unavailable memory set (see above paragraph 10 and Parady Col.4 lines 8-12).

Here, the round robin counter updates at every thread switch, and thus when a thread switch instruction executes and changes to a known level, the thread is switched and the context is swapped out to the unavailable memory set (see above paragraph 42 and Waldspurger paragraphs 2-5 of Sec. 2.2).

45. Claim 11-12, 14 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady in view of Waldspurger as applied to claim 8 above, and further in view of Gillepsie, U.S. Patent No. 6,269,391.

46. Regarding claim 11, Parady in view of Waldspurger has taught the execution unit of claim 8, but have not explicitly taught wherein execution of the context swap instruction specifies an inter-thread signal input and upon receipt of the specified inter-thread signal causes the swapped out thread to be stored in the available memory set.

47. However, Gillepsie has taught a yield instruction which will perform a context change when it receives the signal from a higher-priority thread (see Col.4 lines 35-39) so that events such as time-outs can be properly handled and so a determination of which thread to execute can be made so that problems such as cache thrashing and deadlock can be avoided (see Col.1 lines 37-52 and Col.3 lines 34-46). One of ordinary skill in the art would have recognized that avoiding such problems are beneficial to a microprocessor, preventing time-wasting delays, thereby increasing processing throughput and speed. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady in view of Waldspurger to specify an inter-thread signal which causes a context switch in order to prevent delay problems caused by time-outs.

48. Regarding claim 12, Parady in view of Waldspurger has taught the execution unit of claim 8, but have not explicitly taught wherein the execution of the context swap instruction specifies a voluntary swap operation and causes a context swap if there is a thread in the available memory set ready to be executed.

49. However, Gillepsie has taught a yield instruction which voluntarily relinquishes control of the its thread and performs a context switch to the next available thread (see Col.4 lines 24-58) so that events such as time-outs can be properly handled and so a determination of which thread to execute can be made so that problems such as cache thrashing and deadlock can be avoided (see Col.1 lines 37-52 and Col.3 lines 34-46). One of ordinary skill in the art would have recognized that avoiding such problems are beneficial to a microprocessor, preventing time-wasting delays, thereby increasing processing throughput and speed. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady in view of Waldspurger to specify a voluntary swap operations which causes a context switch in order to prevent delay problems caused by time-outs.

50. Regarding claims 14 and 27, taking claim 14 as exemplary, Parady in view of Waldspurger has taught the execution unit of claim 8, but has not explicitly taught wherein the context event switching logic further comprises:

a. A ctx_enable register and with execution of the context swap instruction specifying a kill operation causing the ctx_enable bit to be set to indicate that this thread is not available for execution until the bit is cleared by another instruction.

51. However, Gillepsie has taught where an instruction can suspend the execution of a thread (see Col.4 lines 44-49) and subsequently request the next available thread, and not allowing the

suspended thread to execute until its start executable field of its associated thread control object is set back to ready (see Col.7 lines 42-55) so that threads which are not ready to execute are not executed. One of ordinary skill in the art would have recognized that properly executing threads are desirable so that erroneous results aren't computed. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady in view of Waldspurger to include logic that has a "start executable" field determining when a thread is ready, a field that is queried when performing a context switch so that only threads that are ready can be executed, thereby preventing erroneous results.

52. Claim 27 is nearly identical to claim 14, differing in its parent claim, but encompassing the same scope. Therefore, claim 27 is rejected for the same reasons as claim 14.

53. Claims 13 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady in view of Waldspurger as applied to claim 8 above, and further in view of Trauben et al., U.S. Patent No. 5,509,130.

54. Regarding claims 13 and 26, taking claim 13 as exemplary, Parady in view of Waldspurger has taught the execution unit of claim 8, but have not explicitly taught wherein execution of the context swap instruction specifies a defer_one operation which causes execution of one more instruction and then causes the current context to be swapped out.

55. However, Trauben has taught a branch delay instruction which causes the execution of one instruction before changing context in order to hide the latency of computing and fetching the branch target (see Col.14 lines 41-60). One of ordinary skill in the art would have recognized that it is desirable to reduce the amount of delay in a microprocessor and thus allow faster execution times. Therefore, one of ordinary skill in the art would have found it obvious to

modify the processor of Parady in view of Waldspurger to include a branch delay instruction which allows an instruction to execute while computing and fetching a branch target so that the latency of the operation can be avoided.

56. Claim 26 is nearly identical to claim 13, differing in its parent claim, but encompassing the same scope. Therefore, claim 26 is rejected for the same reasons as claim 13.

Conclusion

57. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

58. Levy et al., U.S. Patent No. 6,092,175, has taught a multithreaded processor which provides register windowing for each process.

59. Jung et al., "Flexible Register Window Structure for Multi-Tasking", has taught a processor with a relatively addressable banked register file and the ability to multi-task using register windowing.

60. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 7:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

61. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
3/4/2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100